

What is claimed is:

- 1 1. A method, comprising:
2 executing a first thread requiring a first valid virtual memory address representing a first
3 physical memory address;
4 searching a translation look-aside buffer for the first valid virtual memory address;
5 retrieving a first translation upon failing to find the first valid virtual memory address;
6 searching the translation look-aside buffer for the first physical memory address; and
7 overwriting a second translation in the translation look-aside buffer corresponding to the
8 first physical memory address with the first translation.
- 1 2. The method of claim 1, further comprising executing a second thread requiring a third
2 translation corresponding to the first physical memory address.
- 1 3. The method of claim 2, wherein a multithreaded processor executes the first thread and
2 the second thread.
- 1 4. The method of claim 3, wherein the multithreaded processor executes the first thread and
2 the second thread using switch on event multithreaded processing.
- 1 5. The method of claim 3, wherein the multithreaded processor executes the first thread and
2 the second thread using simultaneous multithreaded processing.

1 6. The method of claim 5 further comprising:
2 appending a first set of access rights for the first thread upon overwriting the second
3 translation; and
4 appending a second set of access rights for the second thread upon overwriting the first
5 translation.

1 7. The method of claim 6 further comprising:
2 erasing the first set of access rights if the third translation does not match the first
3 translation.

1 8. The method of claim 7 wherein a content addressable memory is used to search the
2 translation look-aside buffer.

1 9. The method of claim 1 further comprising:
2 creating a first one-hot index associated with the first physical memory address; and
3 validating the first valid virtual memory address using the first one-hot index.

1 10. A set of instructions residing in a storage medium, said set of instructions capable of
2 being executed by a storage controller to implement a method for processing data, the method
3 comprising:
4 executing a first thread requiring a first valid virtual memory address representing a first
5 physical memory address;
6 searching a translation look-aside buffer for the first valid virtual memory address;

7 retrieving a first translation upon failing to find the first valid virtual memory address;
8 searching the translation look-aside buffer for the first physical memory address; and
9 overwriting a second translation in the translation look-aside buffer corresponding to the
10 first physical memory address with the first translation.

1 11. The set of instructions of claim 10, further comprising executing a second thread
2 requiring a third translation corresponding to the first physical memory address.

1 12. The set of instructions of claim 11, wherein a multithreaded processor executes the first
2 thread and the second thread.

1 13. The set of instructions of claim 12, wherein the multithreaded processor executes the first
2 thread and the second thread using switch on event multithreaded processing.

1 14. The set of instructions of claim 12, wherein the multithreaded processor executes the first
2 thread and the second thread using simultaneous multithreaded processing.

1 15. The set of instructions of claim 14, further comprising:
2 appending a first set of access rights for the first thread upon overwriting the second
3 translation; and
4 appending a second set of access rights for the second thread upon overwriting the first
5 translation.

- 1 16. The set of instructions of claim 15, further comprising:
2 erasing the first set of access rights if the third translation does not match the first
3 translation.
- 1 17. The set of instructions of claim 16, wherein a content addressable memory is used to
2 search the translation look-aside buffer.
- 1 18. The set of instructions of claim 10, further comprising:
2 creating a first one-hot index associated with the first physical memory address; and
3 validating the first valid virtual memory address using the first one-hot index.
- 1 19. A processor, comprising:
2 a translation look-aside buffer to store a first translation corresponding to a first physical
3 memory address;
4 a memory execution engine to execute a first thread to search the translation look-aside
5 buffer for the first physical memory address and to overwrite the first translation with a second
6 translation corresponding to the first physical memory address.
- 1 20. The processor of claim 19, wherein the memory execution engine executes a second
2 thread requiring a third translation corresponding to the first physical memory address.

1 21. The processor of claim 20, wherein the memory execution engine executes the first
2 thread and the second thread using switch on event multithreaded processing.

1 22. The processor of claim 20, wherein the memory execution engine executes the first
2 thread and the second thread using simultaneous multithreaded processing.

1 23. The processor of claim 22, wherein the memory execution engine appends a first set of
2 access rights for the first thread upon overwriting the first translation; and appends a second set
3 of access rights for the second thread upon overwriting the second translation.

1 24. The processor of claim 23, wherein the multithreaded processor erases the first set of
2 access rights if the third translation does not match the second translation.

1 25. The processor of claim 19, further comprising a content addressable memory to search
2 the translation look-aside buffer.

1 26. The processor of claim 19, wherein the translation look-aside buffer contains a first one-
2 hot index associated with the first physical memory address to validate the first valid virtual
3 memory address.

1 27. A system, comprising:
2 a memory unit with data stored at a first physical memory address; and

3 a processor coupled to said memory unit and including a translation look-aside buffer to
4 store a first translation corresponding to the first physical memory address; and a memory
5 execution engine to execute a first thread to search the translation look-aside buffer for the first
6 physical memory address and to overwrite the first translation with a second translation
7 corresponding to the first physical memory address.

1 28. The system of claim 27, wherein the memory execution engine executes a second thread
2 requiring a third translation corresponding to the first physical memory address.

1 29. The system of claim 28, wherein the memory execution engine executes the first thread
2 and the second thread using switch on event multithreaded processing.

1 30. The system of claim 28, wherein the memory execution engine executes the first thread
2 and the second thread using simultaneous multithreaded processing.

1 31. The system of claim 30, wherein the memory execution engine appends a first set of
2 access rights for the first thread upon overwriting the first translation; and appends a second set
3 of access right for the second thread overwriting the second translation.

1 32. The system of claim 31, wherein the multithreaded processor erases the first set of access
2 rights if the third translation does not match the second translation.

1 33. The system of claim 27, further comprising a content addressable memory to search the
2 translation look-aside buffer.

1 34. The system of claim 27, wherein the translation look-aside buffer contains a first one-hot
2 index associated with the first physical memory address to validate the first valid virtual memory
3 address.